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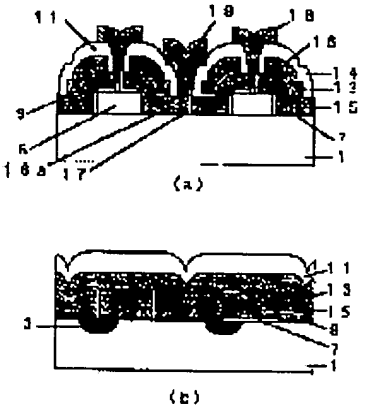
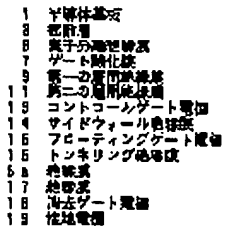
(54) SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To suppress increase in capacitance between floating gates of different memory cells of a floating gate type semiconductor memory device and in particular, secure a reading operation margin of the memory, while miniaturization of the device is realized.
SOLUTION: This floating gate type semiconductor memory device has element isolation insulating films 6 in every other cells among respective memory cells and erasing gate electrodes 18 formed on the element isolation insulating films 6. A ground electrode 19, whose potential is fixed to ground potential, is provided so as to be brought into contact with side surfaces of two floating gate electrodes 15 of the adjacent two element isolation insulating films 6 via insulating films 16a, so that the capacitance coupling caused by a capacitance produced in a narrow gap between the floating gate electrodes 15 can be avoided and wrong reading of a memory state can be avoided.





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